In the Specification:

Please replace the paragraph at page 19, lines 11-18 with the following amended paragraph:

As seen in **Figure 4C**, the second dielectric layer **430** is anisotropically etched to expose the barrier layer **22** and provide sidewall ~~spaces~~ spacers **430'** and a gate contact recess. A gate metal may be deposited and patterned, for example, using lift-off techniques, to ~~provided~~ provide the gate contact **444**. The length of the gate contact **444** may be approximately the width of the first ~~dieleetie~~ dielectric layer **424** less twice the thickness of the second dielectric layer **430**. In particular embodiments of the present invention, the first dielectric **424** may have a width of about 0.5 to about 1 μm and the second dielectric **430** may have a thickness of from about 0.1 to about 0.5 μm.